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UNITED STATES PATENT APPLICATION

FOR

CLOCK GENERATION AND DISTRIBUTION IN AN EMULATION SYSTEM

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CLOCK GENERATION AND DISTRIBUTION IN AN EMULATION SYSTEM

FIELD OF THE INVENTION

The present invention relates to emulation systems, and more particularly, the present invention relates to generation and distribution of multiple synchronized clock signals in an emulation system.

BACKGROUND OF THE INVENTION

Prior art clock generation and distribution schemes for emulation systems typically include a base clock signal, circuitry for frequency multiplying or frequency dividing the base clock signal to generate derived clock signals and circuitry for distributing the derived clock signals. The derived clock signals are typically related to the base clock signal by powers of two. For example, the base clock signal may be frequency divided by two and frequency multiplied by two in order to provide three synchronized clock signals having different frequencies. To generate these derived clock signals, dedicated circuitry is provided to generate each derived clock signal. Additional or different clock signals require additional or different circuitry.

Thus, prior art clock generation and distribution schemes are rigid with respect to the number of derived clock signals provided and the relationship of the derived clock signals to the base clock signal. In particular, prior art clock generation and distribution schemes are unworkable for emulation systems that employ many clocks.

When providing multiple clock signals derived from a single base clock signal, the emulation system typically starts, stops and resumes the base clock signal to start, stop and resume emulation. However, derived clock signals may not be in phase with the base clock signal. When the derived clock signals are not in phase with the base clock signal and emulation is stopped, emulation stops with respect to a rising or falling edge of the base clock signal. However, in clock domains operating on derived clock signals

emulation continues until a subsequent derived clock edge. When emulation is resumed, the base clock signal resumes where stopped, however, because the derived clock signals may not be stopped at the same point in time as the base clock signals because the derived clock signals may be out of phase with respect to the base clock signal, the derived clock signals may not resume at the point where emulation was stopped. Therefore, these prior art clock distribution schemes may not provide fully functional start, stop and resume functionality for emulation.

Therefore, what is needed is a clock generation and distribution method and apparatus that allows generation of derived clock signals without specific circuitry for each derived clock frequency that allows derived clock signals to resume where stopped whether or not the derived clock signal is in phase with the base clock signal.

SUMMARY OF THE INVENTION

A method and apparatus for generating one or more derived clock signals is disclosed. In one embodiment, several derived clock signals are generated from a look up table. A counter circuit counts base clock cycles and provides an index to the look up table. Emulation can be stopped by stopping the base clock signal, which stops the derived clock signals at a stopping point in the respective derived clock cycles. The derived clock signals do not continue to a subsequent transition before stopping. Emulation is resumed by resuming the base clock signal, which causes the derived clock signals to resume at the stopping point in the respective derived clock signal cycle.

Derived clock signals can be resumed where stopped whether at an edge or not to continue emulation thus providing more precise emulation. Look up tables also increase ease of synchronization between derived clock signals over the prior art because multiple derived clock signals are generated in parallel by similar circuitry that result in approximately the same delay for each derived clock signal and transients or irregularities that occur in the base clock signal are passed to the derived clock signals. Thus, if distribution networks are designed to reduce or eliminate clock skew, the derived clock signals maintain the desired phase relationships.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is one embodiment of timing generation circuitry for generating derived clock signals according to the present invention.

Figure 2 is one embodiment of timing generation circuitry for generating derived clock signals having a selection circuit according to the present invention.

Figure 3 is one embodiment of look up table entries and corresponding derived clock signals according to the present invention.

Figure 4 is one embodiment of an emulation system in which the present invention may be implemented.

DETAILED DESCRIPTION

A method and apparatus for clock generation and distribution in an emulation system is described. In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to avoid obscuring the present invention.

Briefly, the present invention provides a method and apparatus for generating one or more derived clock signals with a circuit having a look up table. A counter circuit counts base clock cycles and provides an index into the look up table. In one embodiment, a frequency divider circuit can be used between the counter circuit and a base clock signal to provide an intermediate clock signal with a frequency that is less than the frequency of the base clock signal.

By generating derived clock signals with circuits having look up tables, the derived clock frequencies and duty cycles may be modified by changing the entries in the look up table rather than changing the hardware that provides the derived clock signals as in the prior art thus providing greater flexibility. Additionally, derived clock signals may be resumed where stopped whether at an edge or not to continue emulation thus providing more precise emulation. Look up tables also increase ease of synchronization between derived clock signals over the prior art because multiple derived clock signals are generated in parallel by similar circuitry that result in approximately the same delay for each derived clock signal and transients or irregularities that occur in the base clock signal are passed to the derived clock signal(s).

In one embodiment, a selection circuit is provided to select between the base clock signal and an external clock signal. The external clock signal can be, for example, a derived clock signal from another circuit, an alternative base clock signal, or any other

timing signal. The selection circuit can also include a frequency multiplier to multiply the external clock signal.

Overview of Clock Generation Circuitry

Figure 1 is one embodiment of clock generation circuitry according to the present invention. Derived clock generation circuit 150 receives a base clock signal from base clock generation circuit 100 to generate a derived clock signal. Base clock generation circuit 100 may be a high frequency oscillator, such as a crystal, or any type of circuit that generates a clock signal with the desired frequency.

Derived clock generation circuit 150 generally comprises frequency divider circuit 152, counter circuit 154, and look up table 156. Frequency divider circuit 152 receives a clock signal from base clock generation circuit 100 or other source and generates a lower frequency signal as an output. Frequency divider circuit 152 may be any frequency divider circuit known in the art, or any other type of circuit that provides a frequency division function on the base clock signal received. Alternatively, frequency divider circuit 152 can be replaced by a frequency multiplier circuit to produce a higher frequency clock signal.

Counter circuit 154 receives the output of frequency divider circuit 152 and counts cycles of the clock signal output by frequency divider circuit 152. For example, counter circuit 154 may be a 3-bit counter that counts from 0 to 7. Of course, counter circuit 154 may be a different counter circuit, such as a 2-bit, 4-bit, etc. counter, or any other type of counter circuit.

Look up table 156 receives the output of counter circuit 154, which is used to index entries stored in look up table 156. In one embodiment, look up table 156 comprises asynchronous memory. Any memory configuration that provides look up table functionality can be used. In an embodiment with a 3-bit counter, look up table 156 has eight entries, each of which store an output signal level. The output of look up table 156

is one or more derived clock signals. In an embodiment, with a 3-bit counter and eight entries, look up table 156 sequentially and cyclically outputs the entries stored therein.

Figure 2 is one embodiment of clock generation circuitry including selection circuitry according to the present invention. The circuitry of Figure 2 is the same as the circuitry of Figure 1 with the addition of multiplexor 210 and frequency multiplier 220. Multiplexor 210 allows for the selection of external clock signals other than the base clock signal to provide input to derived clock generation circuit 150.

Select signals (not shown in Figure 2) provided to multiplexor 210 can be generated by a central control circuit that provides select signals to multiple multiplexors. Select signals can also be provided by a derived clock generation circuit that is providing an external clock signal to multiplexor 210. Any manner of generating appropriate control signals known in the art may be used.

By providing the ability to select from multiple clock signals for driving derived clock generation circuit 150, the present invention provides greater flexibility for generating derived clock signals then would otherwise be possible.

In one embodiment, frequency multiplier 220 is coupled between an external clock signal and multiplexor 210. Frequency multiplier 220 multiplies the external clock signal by the appropriate factor to compensate for frequency divider circuit 152 and look up table 156 such that one or more of the derived clock signals has a frequency equal to the external clock signal. By multiplying the external clock signals, the circuitry in derived clock generation circuit 150 may be shared by the external clock signal and the base clock signal. However, transients in the external clock signal are passed though derived clock generation circuit 150 to the output signal. This provides the proper relationship between the external clock signal and the derived clock signals regardless of inconsistencies and/or transients in the external clock signal or the base clock signal, and the ability to start, stop and resume the derived clock signal at points in addition to clock edges.

Figure 3 is one embodiment of look up table entries and corresponding derived clock signals according to the present invention. Figure 3 includes four examples of look up table entries in an eight-entry table and corresponding derived clock signals. It is important to note, however, that any size of look up table may be used and any number of derived clock signal may be generated according to the present invention. In one embodiment, the look up table entries of Figure 3 are stored in a single look up table; however, multiple look up tables can be used.

Look up table entries 300 correspond to entries in a look up table, such as look up table 156 (shown in Figure 1). The INDEX entry is the index or address corresponding to a signal level entry. In one embodiment, eight INDEX values labeled 0 through 7 are included in a look up table. Of course, any number of INDEX values may be used. Look up table entries 300 also include CLOCK_1 entries that indicate signal levels for a derived clock signal for each corresponding INDEX value. In one embodiment, a logical 0 corresponds to a low voltage (e.g., 0 V to 0.7 V) and a logical 1 corresponds to a high voltage (e.g., 3 V to 5V). However, alternative entries and voltage levels may also be used.

The INDEX entries correspond to input signals received from counter circuit 154 (shown in Figure 1). As counter circuit 154 counts from 0 to 7 repeatedly, corresponding signal levels are output. Signal 305 corresponds to look up table entries 300. As the input to the look up table changes, the output from the look up table alternates between a high level and a low level. In this embodiment, the output of the look up table matches the output of the frequency divider circuit in the derived clock generation circuit with the look up table.

Look up table entries 310 generate clock signal 315 with a frequency that is one-half of the frequency of look up table entries 300. An output level (CLOCK_2) is maintained for two consecutive inputs to the look up table.

Look up table entries 320 generate clock signal 325 with the same frequency as clock signal 315 with a different duty cycle. Clock signal 325 is low for three counts from the counter circuit and high for one count. Look up table entries 330 generate clock signal 335 with a frequency that is one-half of the frequency of clock signal 315.

Emulation may be stopped, for example, at time t_2, which is a rising edge of CLOCK_1 corresponding to the transition between INDEX values 4 and 5. However, t_2 does not correspond to an edge for the other clock signals of Figure 3. For prior art emulation systems to stop at t_2, emulation typically continues until the first edge subsequent to t_2. Thus, the clock domains corresponding to CLOCK_2, CLOCK_3, and CLOCK_4 may not stop at t_2. For example, CLOCK_2, CLOCK_3, CLOCK_4 stops between t_2 and t_3. When emulation resumes in the prior art, the stopped clock signals resume from the point at which the clock cycles stopped.

In contrast to the prior art, the present invention allows CLOCK_2, CLOCK_3 and CLOCK_4 to stop and resume at t_2 because look up tables are used to generate clock signals. To stop at t_2, INDEX values input to look up tables 300, 310, 320 and 330 are stopped at 4. Each clock signal is stopped at that point and does not proceed to the subsequent transition. To resume the clock signals at t_2, the INDEX values are incremented to 5 and proceed according to desired emulation sequencing.

Overview of an Emulation System Using Derived Clock Signals

Figure 4 is one embodiment of an emulation system in which the present invention may be implemented. Emulation system 40 generally comprises multiple emulation boards interconnected by a bus or other device. Emulation system 40 also includes a timing generation circuit that provides clock signals to other components of emulation system 40.

Emulation system 40 includes multiple emulation boards, such as emulation boards 410 and 420. Emulation boards allow emulation system 40 to emulate hardware designs for testing and debugging purposes. In one embodiment, each emulation board

includes multiple programmable devices (not shown in Figure 4), such as field programmable gate array (FPGA) devices. Emulation boards are interconnected by bus 400. Alternatively, bus 400 may be replaced by a different device that provides interconnection between multiple boards, such as backplanes and interconnecting boards.

Timing generation circuit 450 is also coupled to bus 400. Timing generation circuit 450 provides one or more clock signals to components of emulation system 40. In one embodiment, timing generation circuit 450 comprises eight circuits for generating derived clock signals. Of course, any number of clock signals may be generated by timing generation circuit 450. In one embodiment, timing generation circuit 450 includes derived clock generation circuitry, such as the circuitry discussed above with respect to Figures 2 and 3.

One advantage of generating derived clock signals according to the present invention is that distributed clock signals do not have a phase shift introduced as a result of using multiple clock generation circuits. Thus, if clock distribution paths are designed to reduce or eliminate skew, the derived clock signals remain in phase, which improves emulation as compared to the prior art.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.
